1.	Name of Course/Module	Introduction to Machine Architecture
2.	Course Code	TMA1271
3.	Status of Subject	Core for B.IT Information Technology Management
4.	MQF Level/Stage	Bachelor Degree – MQF Level 6
5.	Version (state the date of the last Senate approval)	June 2012
6.	Requirement for Registration	TCE1111 Digital Systems
7.	Name(s) of academic/teaching staff	Mohd Fikri Azli Bin Abdullah Asrul Hadi b Yaacob Hiew Bee Yan
8.	Semester and Year offered	Trimester 2 (Beta Level)
9.	Objective of the course/module in the programme :	
	This course provides thorough discussions on the fundamentals of computer organization and architecture and relates this to contemporary design issues. This will cover system buses, structures and functions of different central processing units, control units, characteristics and functions of different instruction sets, addressing modes, memory, input/output, parallel processing and multi-core computing.	
10.	Learning Outcomes :	
	At the completion of the subject, students should be able to: LO1: Describe the evolution of computer architectures. (Cognitive, Level 1) LO2: Explain the structures and functions of the computer's primary components. (Cognitive, Level 2) LO3: Construct simple assembly language programs. (Psychomotor, Level 4) LO4: Develop the best solution for computer architecture problems. (Cognitive, Level 5)	
11.	Synopsis:	

	This course will cover historical development of computers and evolution of Intel multi-core processors and IBM power processors. Topics such as elements of system bus design, interrupts, organization of registers (with Intel 8085, Intel 8086, and Motorola 68000 microprocessors as examples), study of instruction cycle and pipelining, study of arithmetic and logic unit with integer and floating-point arithmetic algorithms, study of hardwired and micro-programmed control unit, and study of instruction set characteristics, functions, formats, addressing modes (with Intel 8085 and Intel 8086 as examples) will be included. In addition, the following topics in memory and input/output will also be covered with details: Principles of cache memory and elements of cache design, types and organization of semiconductor main memory, structure and function of input/output modules with different data transfer techniques, and interfacing of Intel 8085/8086 microprocessors with 8255 programmable peripheral interface device. Topics in advanced computer architecture such as symmetric multiprocessors, software/hardware solutions for cache coherence problem, configuration of clusters, organization of non-uniform memory access, and motivation behind multi-core computing with architecture and performance characteristics of different multi-core processors will also be introduced.
	Kursus ini merangkumi sejarah pembangunan komputer dan evolusi pemproses teras-berbilang Intel serta pemproses berdaya tinggi IBM. Topik-topik seperti elemen-elemen rekabentuk sistem, sampukan, organisasi pendaftaran (menggunakan pemproses Intel 8085, Intel 8086 dan Motorola 68000), pembelajaran kitar arahan dan penalian paip, unit logik aritmetik, algoritma aritmetik integer dan titik ampung, mikroatur cara terdawai keras, ciri-ciri arahan set, fungsi, format serta mod pengalamatan berlandaskan pemproses Intel 8085 dan 8086 adalah pengkhususan subjek ini. Topik-topik berteraskan ingatan dan masukan/keluaran juga akan diperkenalkan secara terperinci : Prinsip-prinsip serta elemen rekabentuk ingatan para, kepelbagaian jenis dan organisasi semikonduktor ingatan utama, fungsi-fungsi modul masukan/keluaran dengan kepelbagaian aturcara pemindahan data serta antaramuka pemproses Intel 8085/8086 menggunakan peranti boleh aturcara 8255. Tidak ketinggalan topik-topik lanjutan dalam bidang senibina komputer . Ia meliputi pemproses berbilang simetri, penyelesaian perisian dan perkakasan untuk masalah kekoherenan para, konfigurasi kelompok, organisasi ketidakseragaman akses ingatan, dorongan disebalik pengkomputeran teras-berbilang serta rekabentuk dan ciri-ciri prestasi pelbagai pemproses teras-berbilang.

12. Mapping of Subject to Programme Outcomes :

Programme Outcomes	**% of Contribution**
PO1: Apply soft skills in work and career related activities.	40%
PO2: Demonstrate knowledge and understanding of fundamental concepts, principles and best practices.	60%

13. Assessment Methods and Types :

Method and Type	Description/Details	Percentage
Laboratory		20%
Mid-term Test		20%

	Final Exam		60%

14. Details of Subject

Topics	Mode of Delivery	
	Lecture	Laboratory
1.Introduction Brief History of Computers, Designing for Performance, Pentium and PowerPC Evolution, Computer Component, Computer Functions, Interconnection Structure, Bus Interconnection and PCI.	6	0
2.CPU structure and function Processor Organization, Register Organization, The Instruction Cycle, Instruction Pipelining, The Pentium II and PowerPC processors, Micro-operations, Control of The Processor	6	0
3.Computer Arithmetic The Arithmetic and Logic Unit (ALU), Integer representation, Integer arithmetic, Floating-Point Representation, Floating-Point Arithmetic	6	0
4.Instruction Set Design Machine Instruction Characteristics, Types of Operands, Type of Operations, Pentium II and PowerPC Data Types and Operation Types, Addressing, Instruction Formats, Pentium II and PowerPC Addressing Modes and Instruction Formats.	6	0
5.Memory System Architecture Computer Memory System Overview, Semiconductor Main Memory, Cache Memory, Pentium II and PowerPC Cache Organization, Advanced DRAM Organization.	6	0
6.Input/Output External Devices, I/O Modules, Programmed I/O, Interrupt Driven I/O, Direct Memory Access, I/O Channels and Processors, The External Interface: SCSI and FireWire.	3	0
7.Microprocessor Systems Stored Program Concepts, Architecture of Intel 8085 Microprocessor, Arithmetic Logic Unit and Timing and Control Unit, Address Buffers and Latches, Addressing Modes, Addressing Modes in 8085 Microprocessor, Instruction Set of Microprocessor, Groups of Instructions, Timing Diagram of Microprocessor Instructions, Flag Register Organisation, Assembly Language Programming, Microprocessor Interfacing, I/O Ports, Memory-mapped and I/O Mapped, Address Space Partitioning, Memory Interfacing, Programmable Peripheral Interface (8255), 8279 Keyboard Display Interface.	0	24

	8.Introduction to Advanced Computer Architecture Instruction Execution Characteristics, The Use of a Large Register File, Compiler-Based Register Optimization, Reduced Instruction Set Architecture, RISC Pipelining, The RISC versus CISC Controversy, Multiple Processor Organizations, Symmetric Microprocessors, Cache Coherence and the MESI Protocol, Clusters, Non-uniform Memory Access, Vector Computation.	3	0
	Total	36	**24**

15. Laboratories

- Basic Operation using 8-bit Microprocessor Kits.
- Assembly Language Program for:
  a) Addition, Subtraction, Multiplication and Division of Numbers
  b) Logical Operations
  c) Sorting of Numbers
  d) Serial Input and Output
- Interfacing : Memory and Input/output
- Interfacing: Memory

16.

Total Student Learning Time (SLT)	Face to Face (Hour)	Total Guided and Independent Learning
Lecture	36	36
Tutorials	-	-
Laboratory Exercise	24	12
Presentation	-	-
Assignment	-	-
Mid Term Test	1	5
Lab Test	2	4
Final Exam	2	20
Quizzes	-	-
Sub Total	**65**	**77**
Total SLT	**142/40 = 3.55 => 4**	

17. Credit Value: 4

18. Reading Materials :

Textbook	Reference Materials
1. William Stallings, *"Computer Organization and Architecture",* Seventh Edition, Prentice Hall, 2006.	1. Miles Murdocca , Vincent P. Heuring, *"Principles of Computer Architecture, First Edition"*, Engineering/Science/Mathematics 1999 2. Andrew S. Tanenbaum , *"Structured Computer Organization, Fourth Edition*, Engineering/Science/Mathematics, 1998 3. D. Patterson and J. Hennessy, *"Computer Organization & Design - The Hardware/Software Interface"*, Morgan Kaufmann Publishers, 1994. 4. Gaoengar, *"Microprocessors: Architecture, Programming and Applications"*, John Wiley & Sons, 1995.

19.	Appendix (to be compiled when submitting the complete syllabus for the programme) : 1. Mission and Vision of the University and Faculty 2. Mapping of Programme Objectives to Vision and Mission of Faculty and University 3. Mapping of Programme Outcome to Programme Objectives 4. Program Objective and Outcomes (Measurement and Descriptions)