MULTIMEDIA UNIVERSITY®

COURSE INFORMATION

1.	**Name of Course**	Computer Architecture and Organisation	
2.	**Course Code**	TAO1221	
3.	**Type of Course** **(e.g. : Core, major, elective etc.)**	Common Core for B.IT (Hons) Data Communications and Networking B.IT (Hons) Information Technology Management B.IT (Hons) Artificial Intelligence B.IT (Hons) Security Technology B.Sc (Hons) Bioinformatics	
4.	**Synopsis**	This subject provides introduction to system bus design, interrupts, organization of registers, study of instruction cycle and pipelining, study of arithmetic and logic unit with integer and floating-point arithmetic algorithms, study of hardwired and micro-programmed control unit, and study of instruction set characteristics, functions, formats, addressing modes	
5.	**Version** **(State the date of theSenate's approval - previous and the current approval date)**	Current: Aug 2017 Previous: June 2014	
6.	**Name(s) of Academic Staff**	Mohd Fikri Azli bin Abdullah	
7.	**Semester and Year Offered**	Trimester 2, Year 1	
8.	**Credit Value**	4	
9.	**Pre-Requisite**	None	
10.	**Objective of the course in the programme:**		
	This course provides thorough discussions on the fundamentals of computer organization and architecture and relates this to contemporary design issues. This will cover system buses, structures and functions of different central processing units, control units, characteristics and functions of different instruction sets, addressing modes, memory, input/output, parallel processing and multi-core computing.		
11.	**Justification for including the course in the programme:**		
	This course will cover historical development of computers and evolution of Intel multi-core processors and IBM power processors. Topics such as elements of system bus design, interrupts, organization of registers (with Intel 8085, Intel 8086, and Motorola 68000 microprocessors as examples), study of instruction cycle and pipelining, study of arithmetic and logic unit with integer and floating-point arithmetic algorithms, study of hardwired and micro-programmed control unit, and study of instruction set characteristics, functions, formats, addressing modes (with Intel 8085 and Intel 8086 as examples) will be included		
12.	**Course Learning Outcomes (CLO)**	**Domain**	**Level**
	CLO1: Describe the evolution of computer architectures.	Cognitive	1
	CLO2: Identify and explain the structures and functions of the primary components of computer such as system buses, registers, ALU, control unit, memory, input-output devices and also the characteristics of instructions sets of typical microprocessors.	Cognitive	2
	CLO3: Demonstrate the ability to write simple assembly language programs and also programs for the programmable peripheral interface device with different interfacing techniques.	Cognitive	3

	CLO4: Construct the best solution and organization of single processor systems, symmetric multiprocessors clusters, non-uniform memory access and chip-level multiprocessors in response to problems associated with computer architectures.	Cognitive	3

13. Mapping of the Course Learning Outcomes to the Programme Learning Outcomes, Teaching Methods and Assessment:

Course Learning Outcomes (CLO) (Must tally with CLOs in item 12)	Programme Learning Outcomes (PLO)												Teaching Methods	Assessment Method
	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10	PLO11	PLO12		
CLO1	✓												Lecture/Lab	Written Test /Final/ Lab submission
CLO2		✓											Lecture/ Lab	Written Test /Final/ Lab submission
CLO3							✓						Lecture/ Lab	Written Test /Final/ Lab submission
CLO4								✓					Lecture/ Lab	Written Test /Final/ Lab submission
Total	**1**	**1**					**1**	**1**					*Indicate the relevancy between the CLO and PLO by ticking "□" the appropriate relevant box (This description must be read together with standards 2.1.2, 2.2.1, and 2.2.2 in Area 2 – pages 16 & 18 of COPPA 2.0)*	

14. Transferable Skills:

Teamwork, Problem solving and Technical skills

15. Distribution of Student Learning Time (SLT)

Course Content Outline	**CLO	Teaching and Learning Activities – Guided Learning (F2F)*				Guided Learning (NF2F)*	Independent Learning (NF2F)*	Total SLT
		*L	*T	*P	*O			
1 Introduction Brief History of Computers, Designing for Performance, Pentium and PowerPC Evolution, Computer Component, Computer Functions, Interconnection Structure, Bus Interconnection and PCI	**CLO 1**	6		4	1		11	22
2 CPU structure and function Processor Organization, Register Organization, The Instruction Cycle, Instruction Pipelining, processors, Micro-operations, Control of The Processor	**CLO 2**	6		4	1		11	22
3 Computer Arithmetic The Arithmetic and Logic Unit (ALU), Integer representation, Integer arithmetic, Floating-Point Representation, Floating-Point Arithmetic	**CLO 2**	6		4	1		11	22

	4 Instruction Set Design Machine Instruction Characteristics, Types of Operands, Type of Operations, Data Types and Operation Types, Addressing, Instruction Formats, Processor Addressing Modes and Instruction Formats	**CLO 3**	6		4	1		11	22
	5 Memory System Architecture Computer Memory System Overview, Semiconductor Main Memory, Cache Memory, Cache Organization, Advanced DRAM Organization	**CLO 2**	4		4	1		9	18
	6 Input/ Output External Devices, I/O Modules, Programmed I/O, Interrupt Driven I/O, Direct Memory Access, I/O Channels and Processors, The External Interface.	**CLO 3**	4		4			8	16
	7 Introduction to Advanced Computer Architecture Multiple Processor Organizations, Symmetric Microprocessors, Cache Coherence and the MESI Protocol, Clusters, Non-uniform Memory Access.	**CLO 4**	4		2			6	12
								Total SLT	**134**

SUMMATIVE ASSESSMENT

1. Continuous Assessment	**Percentage %**	**Total SLT**
Lab submissions	25%	
Written test	25%	6
Total SLT for Continuous Assessment		**6**

2. Final Assessment	**Percentage %**	**Total SLT**	
		F2F	**ILT**
Final Exam	50%	2	18
Total SLT for Final Assessment (F2F + NF2F)		**20**	
Grand Total	**100%**	**160**	

****Indicate the CLO based on the CLO's numbering in Item 12.**
***L= Lecture, *T= Tutorial, *P= Practical, *O= Others, F2F*= Face to Face, NF2F*= Non Face to Face**

16. **Identify Special Requirement to Deliver the Course (e.g., software, nursery, computer lab, simulation room):**

17. **Main References:**

William Stallings, (2016). Computer Organization and Architecture, 10th Edition, Prentice Hall

18. **Additional References:**

Miles Murdocca, Vincent P. Heuring, (1999). Principles of Computer Architecture, First Edition, Engineering/Science/Mathematics.
Andrew S. Tanenbaum, (2012). Structured Computer Organization, Sixth Edition, Engineering/Science/Mathematics.
Patterson, D. and Hennessy, J. (2013). Computer Organization & Design - The Hardware/Software Interface, 5th Ed., Morgan Kaufmann Publishers.
Gaoengar, (2002). Microprocessors: Architecture, Programming and Applications with 8085, 5th Ed., John Wiley & Sons.

Note:

	Cells shaded light grey contain formulas / fixed values. Edit these formulas only if needed.